ADVANCE TECHNICAL PROGRAM

1st IEEE Federative Event on Design for Robustness
FEDfRo

Hotel Eden Roc, Sant Feliu de Guixols, Catalunya, Spain
July 4-6, 2016
http://tima.imag.fr/conferences/fedfro/fedfro16/

Nanometer scaling and the related aggressive reduction of device geometries steadily worsens noise margins; process, voltage and temperature variations; aging and wear-out; soft error and EMI sensitivity; power density and heating; and make mandatory the use of efficient techniques for improving yield and reliability, extending lifespan, and reducing power dissipation of modern SoCs. Additionally, the rapidly increasing complexity of modern SoCs further aggravates these issues, and makes it extremely difficult to guarantee that the design of these chips meet their specifications.
Furthermore, the pervasiveness of electronic systems in modern societies, and their ubiquitous implication in all aspects of our everyday lives, drastically raises the requirements to protect modern electronic systems against all these threats, as well as versus those induced by intentional attacks against their security.
These trends have made mandatory the development of efficient Design for Robustness approaches for mitigating these pluralities of threats. However, as DfX techniques are proliferating (**Design for Test, Design for Debug, Design for Yield, Design for Reliability, Design for Low-Power, Design for Security, Design for Verification**, …), it becomes mandatory to address these issues holistically, in order to moderate their impact on area, power, and/or performance, and increase their global efficiency. There is therefore a related need for an international consolidated forum bringing together specialists from all these domains to enhance interactions and cross-fertilization. **FEDfRo**, sponsored by the IEEE Council on Electronic Design Automation (CEDA), was initiated to meet this goal by bringing together:

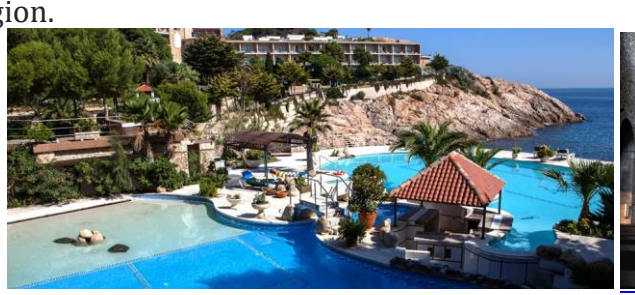
- **IOLTS: the 22nd International Symposium on On-Line Testing and Robust System Design** ***http://tima.imag.fr/conferences/iolts/iolts16***
- **IMSTW: the 21st International Mixed-Signal Testing Workshop** ***http://tima.imag.fr/conferences/imstw/imstw16***
- **IVSW: the 1st International Verification and Security Workshop** ***http://tima.imag.fr/conferences/ivsw/ivsw16***

Those events will be held in the same location and will run in parallel. To encourage interactions, **participants registered in any one of the events can freely attend sessions of the other two events.**
All social activities will also be done jointly to increase interactions among attendees.

About the location: FEDfRo 2016 will be held at **Sant Feliu de Guixols**, Costa Brava, Spain. The area offers a brilliant experience, with so much to offer: a beautiful natural setting, culture, leisure, sport, and a delightful seafront location with a multitude of idyllic small coves and longer bays with fine and golden sand …
Sant Feliu de Guixols has also an impressive monumental site, formed by the parish church and different elements from the Romanesque monastery of the village, with its famous Porta Ferrada.
Sant Feliu de Guixols is close to the main communication routes, in the Costa Brava area, and is situated at:

- 32 km from Girona Airport (33 min by car).
  Private door-to-door transportation between Girona Airport and Sant Feliu de Guixols: 47 €.
- 118 km from Barcelona Airport (1 hour 23 min by car).
  Bus company Sarbus ensures 14 daily trips between Barcelona Airport and Sant Feliu de Guixols: 17 € cost, about 2 hours trip.
- 108 km from Barcelona (1 hour 22 min by car).
- 80 km from Figueres: birthplace Salvador Dalí, housing the **Dalí Theatre-Museum** considered as the largest surrealistic object in the world.
- 98 km from the French borders.
- 281 km from Montpellier, France (2 hours 59 min by car).

The Venue: FEDFRo 2016 will be held at the hotel Eden Roc, located at a 1 km from Sant Feliu de Guixols, and 8 minutes walking distance from the main golden sandy beach of the town. **Eden Roc** is built on the seafront rocks of a unique and quiet peninsula, **enjoying stunning sea views,** and is situated at few meters from the seafront, with its nice terraces, gardens, and swimming pools touching the sea.
Along the coast in either direction are a multitude of small coves and longer bays with fine sand and many services. You can spend your entire holiday on a different beach every day.
The hotel amenities include among others, freshwater and seawater outdoor swimming pools, heated indoor swimming pool, comfortable lounges, elegant living rooms, 2 bars, own bridge and billiards room, health center, massage service, hot tubs, 2 restaurants with abundant barbecue buffet at noon and in the evening a buffet with elected specialties of the region.



IEEE CEDA IEEE Council on Electronic Design Automation tttc

Monday July 4, 2016

08:00 – 09:00: Registration

09:00 – 10:00: FEDfRo Plenary Session

Conference Room: Mediterraneo

- Welcome Message by General Chairs of IOLTS, IMSTW and IVSW
- **FEDfRO Keynote Talk:** Dr. Karim Arabi, VP of R&D, Qualcomm,

Driving opportunities and technical challenges of the next wave of semiconductor devices

10:00 – 10:15: Break

22nd IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS)

Conference Room: Mediterraneo

10:15 – 11:15: IOLTS Opening Session

- **Symposium Introduction**
  M.Nicolaidis (TIMA Lab), General Chair
  D.Gizopoulos (U Athens), D.Alexandrescu (iRoC), Program Chairs
- **IOLTS Keynote Talk:** Franz Dietz (Bosch)
  Starting the journey towards resilient automotive electronics,

11:15 – 11:30: Coffee Break

11:30 – 12:30: Session 1 – Posters

- **On the robustness of DCT-based compression algorithms for space applications**
  S.Avramenko, M.Sonza Reorda, M.Violante (Politecnico di Torino), G.Fey (U Bremen / DLR), J.-G.Mess, R.Schmidt (DLR)
- **Analytic Models for Crossbar Read Operation**
  A.Adeyemo, X.Yang, A.Bala (Oxford Brookes U), J.Mathew (IIT Patna), A.Jabir (Oxford Brookes U)
- **A Fault-tolerant Sequential Circuit Design for SAFs and PDFs Soft Errors**
  A.Matrosova, S.Ostanin, I.Kirienko, E.Nikolaeva (Tomsk State U)
- **ACM: Accurate Crosstalk Modeling to Predict Channel Delay in Network-on-Chips**
  Z.Mahdavi, Z.Shirmohammadi, S.G.Miremadi (Sharif U Technology)
- **An On-Line Test Solution for Addressing Interconnect Shorts in on-Chip Networks**
  B.Bhowmik, J.K.Deka, S.Biswas (IIT Guwahati)
- **An Soft Error Propagation Analysis Considering Logical Masking Effect on Re-convergent Path**
  S.Yoshida, G.Matsulawa, S.Izumi, H.Kawaguchi, M.Yoshimoto (Kobe U)
- **Analysis of BTI Aging of Level Shifters**
  J.Cai, B.Halak, D.Rossi (U Southampton)
- **Cache-aware Reliability Evaluation through LLVM-based Analysis and Fault Injection**
  M.Kooli, G.Di Natale, A.Bosio (LIRMM)
- **Comparison of RTL Fault Models for the Robustness Evaluation of Aerospace FPGA devices**
  V.Beroulle, R.Champon, A.Papadimitriou (Grenoble Alpes U), D.Hely (Grenoble INP), G.Genevrier, F.Cezilly (Thales)
- **Efficient Fault-tolerant Parallel Matrix-Vector Multiplications**
  Z.Gao (Tianjin U), P.Reviriego, J.-A.Maestro (U Antonio de Nebrija)

12:30 – 13:45: Lunch

13:45 – 14:45: Session 2 – Robust Memories

Moderator: A.Grasset (Thales)

- **Resilient Random Modulo Cache Memories for Probabilistically-Analyzable Real-Time Systems**
  D.Trilla, C.Hernandez, J.Abella (BSC), F.J.Cazorla (BSC, IIIA-CSIC)
- **Statistical Analysis and Comparison of 2T and 3T1D e-DRAM Minimum Energy Operation**
  M.Rana, R.Canal, E.Amat, A.Rubio (UPC)
- **Variations-Tolerant 9T SRAM Circuit with Robust and Low Leakage SLEEP Mode**
  H.Jiao, Y.Qiu (Eindhoven U of Technology), V.Kursun (The Hong Kong U of Science and Technology)

14:45 – 15:00: Break

15:00 – 16:00: Special Session 1 – EDA Support for Functional Safety

Organizer/Moderator: D.Alexandrescu (iRoC)

- **How EDA can Improve Productivity in the Assessment of Functional Safety**
  D. Alexandrescu, iRoC
- **Infrastructure IP of SOCs in Automotive Applications** Y. Zorian, Synopsys
- **Title** and Presenter TBA

16:00 – 16:30: Coffee Break

21st IEEE International Mixed Signal Testing Workshop (IMSTW)

Conference Room: Goya

10:15 – 11:15: IMSTW Opening Session

- **IMSTW Opening Message**
- **IMSTW Keynote Talk:** Abhijit Chatterjee, Georgia Tech
  Self-aware communication and control systems: multi-dimensional adaptation for variability, induced errors and performance

11:15 – 11:30: Coffee Break

11:30 – 12:30: Special Session 1: Sensors for test and test instruments –Part 1

Organizer/Moderator: H. Stratigopoulos (LIP6)

- **Taxonomy and challenges of the integration of power supply monitors**
  Pablo Ituero, Universidad Politécnica de Madrid, Spain
- **BIST of power and control lines in CMOS imagers** Salvador Mir, TIMA, France

12:30 – 13:45: Lunch

13:45 – 14:45: Invited talks 1

Moderator: S. Mir (TIMA)

- **Efficient Calibration of Contact-less Resonant Bio-sensor Affected by Operating Conditions**
  Anthony Deluthault, Vincent Kerzérho, Serge Bernard, Fabien Soulier, LIRMM, France, Philippe Cauvet, Ophtimalia, France
- **Characterization of temperature sensors using Peltier cells**
  João F. M. Ventura, IST – UTL / INESC-ID, Portugal, Tiago H. Moita, INESC-ID, SILICONGATE LDA, Portugal, Marcelino B. Dos Santos, IST – UTL / INESC-ID, SILICONGATE LDA, Portugal

14:45 – 15:00: Break

15:00 – 16:00: Regular session 1

Moderator: M. Renovell (LIRMM)

- **Successive Approximation Time-to-Digital Converter with Vernier-level Resolution**
  Richen Jiang, Congbing Li, Mingcong Yang, Haruo Kobayashi, Yuki Ozawa, Nobukazu Tsukiji, Mayu Hirano, Kazumi Hatayama, Gunma University, Japan, Ryoji Shiota, Socionext Inc., Japan
- **A Multi-Channel FPGA-Based Time-to-Digital Converter**
  Ling-Yun Hsu, Jiun-Lang Huang, National Taiwan University, Taiwan

16:00 – 16:30: Coffee Break

1st IEEE International Verification and Security Workshop (IVSW)

Conference Room: Port Salvi

10:15 – 11:15: Session 1 - IVSW Opening Session

- **IVSW Opening Message**
- **IVSW Keynote Talk:** Dr. Swarup Bhunia, University of Florida,
  Where Security Meets Verification: From Microchip to Medicine

11:15 – 11:30: Coffee Break

11:30 – 12:30: Session 2 – Hardware Security Assurance

Moderator: Ilia Polian, U. Passau

- **Tools and Development Environments for Hardware Security Assurance throughout Product Life Cycle: Past, Present, and Future**
  Sohrab Aftabjahani, Intel
- **Physical Unclonable Functions: Un-Trusted Silicon is not an option**
  Pim Tuyls, Intrinsic ID

12:30 – 13:45: Lunch

13:45 – 14:45: Session 3 – Hardware Security Implementations

Moderator: Swarup Bhunia, U. Florida

- **Protection of ECC Computations against Side-Channel Attacks for Lightweight Implementations**
  Thibaud Backenstrass, Mathieu Blot, Simon Pontié and Regis Leveugle, Univ. Grenoble Alpes
- **RRAM Based Cell for Hardware Security Applications**
  Daniel Arumi, Rosa Rodriguez-Montañés and Salvador Manich, UPC

14:45 – 15:00: Break

15:00 – 16:00: Session 4 - New Emerging Threats

Moderator: Sohrab Aftabjahani, Intel

- **Hardware Trojans in early design steps: An emerging threat**
  Ilia Polian, University of Passau
- **Resiliency and Trust in Near Threshold Computing**
  Mehdi Tahoori, University of Karlsruhe

16:00 – 16:30: Coffee Break

16:30 – 17:30: Special Session 2 – Aging Modeling and Mitigation

Organizer: Florian Cacho, STMicroelectronics

- **Hot-Carrier and BTI Damage Distinction for High Performance Digital Application in 28nm FDSOI and 28nm LP CMOS nodes**
  A. Bravaix, M. Saliva, F. Cacho, X. Federspiel, C. Ndiaye, S. Mhira, E. Kussener, E. Pauly, V. Huard
- **Activity Profiling: review of different solutions to develop reliable and performant design**
  F. Cacho, A. Benhassain, S. Mhira, A. Sivadasan, V. Huard, P. Cathelin, V. Knopik,A. Jain, C. Parthasarathy, L. Anghel
- **Fine-grain analysis of the parameters involved in aging of digital circuits**
  Boukary Ouattara, Olivier Heron, Chiara Sandionigi

17:30 – 17:45: Break

17:45 – 18:45: Session 3 – "To Inject or not to Inject?"

Moderator: A.Paschalis (U Athens)

- **Evaluating Application-Aware Soft Error Effects in Digital Circuits without Fault Injections or Probabilistic Computations**
  K.Chibani, M.Portolan, R.Leveugle (TIMA Laboratory)
- **Modeling RTL Fault Models Behavior to Increase the Confidence on TSIM-based Fault Injection**
  J.Espinosa (UPV), C.Hernandez (BSC), J.Abella (BSC)
- **Revisiting Software-based Soft Error Mitigation Techniques via Accurate Error Generation and Propagation Models**
  M.Ebrahimi, M.Rashvand (Karlsruhe Institute of Technology), F.Kaddachi (LIRMM), M. Tahoori (Karlsruhe Institute of Technology), G.Di Natale (LIRMM)

18:45 – 19:00: Break

19:00 – 20:00: Session 4 – Validation and Verification

Moderator: S.Hellebrand (U Paderborn)

- **ISA-Independent Post-Silicon Validation for the Address Translation Mechanisms of Modern Microprocessors**
  G.Papadimitriou, A.Chatzidimitriou, D.Gizopoulos (U Athens), R.Morad (IBM Research Labs)
- **Flexible in-Silicon Checking of Run-Time Programmable Assertions**
  Y.Zhou, O.Bringmann, W.Rosenstiel (U Tuebingen)
- **Hardware-Simulation Correlation of Timing Error Detection Performance of Software-based Error Detection Mechanisms**
  Y.Masuda, M.Hashimoto, T.Onoye (Osaka U)

16:30 – 18:00: Special Session 2: Security

Organizer: K. Huang (SDSU)

Moderator: J. Figueras (UPC)

- **Targeting Hardware Trojans in Mixed-Signal Circuits for Security**
  Abhijit Chatterjee, Georgia Tech, USA
- **Security aspects of analog and mixed-signal circuits**
  Ilia Polian, Univ. Passau, Germany
- **Randomness in emerging technologies: functional robustness vs. security**
  Elena Ioana Vatajelu, Politecnico di Torino, Italy

18:00 – 18:15: Break

18:15 – 19:45: Invited talks 2

Moderator: G. Léger (IMSE-CNM)

- **Statistically enhanced analog and Mixed-Signal design and test**
  P. Lima Ramos, Faculty of Engineering, University of Porto, Portugal, J. Machado da Silva, INESC TEC, and Faculty of Engineering, University of Porto, Portugal
- **Post-Silicon Validation of Analog/Mixed-Signal/RF Circuits and Systems: Recent Advances**
  Abhijit Chatterjee, Sabyasachi Deyati, Barry Muldrey, Georgia Tech, USA
- **Using Distortion Shaping Technique to Equalize ADC THD Performance Between ATEs**
  Peter Sarson, ams AG, Austria, Haruo Kobayashi, Gunma University, Japan

16:30 – 17:30: Session 5 – Innovative Verification Methods

Moderator: D. Hely, U. Grenoble Alpes

- **New Architecture of the Object-Oriented Functional Coverage Mechanism for Digital Verification**
  Marek Cieplucha and Witold Pleskacz, Warsaw University of Technology
- **Simulation-based verification of large-integer arithmetic circuits**
  Nejmeddine Alimi and Younes Lahbib Faculty of Sciences of Tunis University

17:30 – 17:45: Break

17 :45 – 18:45: Session 6 – Test and Security Implications

Moderator: Mehdi Tahoori, U. Karlsruhe

- **Manufacturing Test of Secure Devices**
  Giorgio Di Natale, LIRMM
- **Strict Avalanche Criterion and its Implications on PUF Security**
  Rajat Subhra Chakraborty, IIT Kharagpur, India

20:00: Welcome Reception

Tuesday July 5, 2016

22nd IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS)

Conference Room: Mediterraneo

09:00 – 10:00: Session 5 – Degradation

Moderator: S.Di Carlo (Politecnico di Torino)

- **On-line Write Margin Estimator to Monitor Performance Degradation in SRAM Cores**
  B.Alorda, C.Carmona, G.Torrens, S.Bota (U Illes Balears)
- **Recovery of Performance Degradation in Defective Branch Target Buffers**
  F.Filippou, G.Keramidas, M.Mavropoulos, D.Nikolos (U Patras)
- **NBTI Aging Evaluation of PUF-based Differential Architectures**
  M.S.Mispan, B.Halak, M.Zwolinski (U Southampton)

10:00 – 10:15: Break

10:15 – 11:15: Session 6 – Fault Tolerance Techniques

Moderator: M.Violante (Politecnico di Torino)

- **REMO: Redundant Execution with Minimum Area, Power, Performance Overhead Fault Tolerant Architecture**
  S.Gopalakrishnan, V.Singh (IIT Bombay)
- **Susceptible-Workload driven Selective Fault Tolerance using a Probabilistic Fault Model**
  M.Gutierrez, V.Tenentes, T.Kazmierski (U Southampton)
- **Temperature- and Aging-Resistant Inverter for Robust and Reliable Time to Digital Circuit Designs in a 65nm Bulk CMOS Process**
  K.Tscherkaschin, T.Hillebrand, M.Taddiken, S.Paul, D.Peters-Drolshagen (U Bremen)

11:15 – 11:30: Coffee Break

11:30 – 12:30: Special Session 3 – Advanced Fault Tolerant Techniques for Reliability and Low-Power

Organizer: Michael Nicolaidis, TIMA

- **Leakage mitigation for low power microcontroller design in 40nm for internet-of-things (IoT)**
  Ajay Kapoor, Nur Engin, Johan Verdaasdonk, NXP
- **Advanced Double-Sampling Architectures**
  Michael Nicolaidis, Michael Dimopoulos, TIMA
- **Pushing the Limits: How Fault Tolerance Extends the Scope of Approximate Computing**
  Hans-Joachim Wunderlich, Claus Braun, Alexander Schöll

12:30 – 13:45: Lunch

13:45 – 14:45: Session 7 – Soft Errors Mitigation

Moderator: R.Velazco (TIMA)

- **Tackling Long Duration Transients in Sequential Logic**
  E.Koser, W.Stechele (TU Munich)
- **HLS-based Sensitivity-Inductive Soft Error Mitigation for Satellite Communication Systems**
  X.Chen (Sun Yat-sen U), W. Yang (BCIA), M.Zhao, J.WANG (Tsinghua U)
- **An Efficient LDPC Encoder Architecture for Space Applications**
  D.Theodoropoulos, A.Paschalis, N.Kranitis (U Athens)

21st IEEE International Mixed Signal Testing Workshop (IMSTW)

Conference Room: Goya

09:00 – 10:00: Regular session 2:

Moderator: J.L. Huang (National Taiwan U.)

- **Timing Measurement BOST Architecture with Full Digital Circuit and Self-Calibration Using Characteristics Variation Positively for Fine Time Resolution**
  Congbing Li, Junshan Wang, Haruo Kobayashi, Gunma University, Japan, Ryoji Shiota, Socionext Inc., Japan
- **Design Trade-offs for On-chip Driving of High-speed High-performance ADCs in Static BIST Applications**
  Antonio Jose Gines, Eduardo Peralías, Gildas Leger, Adoracion Rueda, IMSE-CNM, CSIC-Universidad de Sevilla, Spain, Guillaume Renaud, Manuel Jose Barragan, Salvador Mir, TIMA, France

10:00 – 10:15: Break

10:15 – 11:15: Session 8 – Panel: DFT vs. Security – Is it a Contradiction? How Can We Get the Best of Both Worlds

Moderator: Magdy Abadir

Panelists: Sohrab Aftabjahani (Intel), Swarup Bhunia (UFL), Giorgio Di Natale (LIRMM), Regis Leveugle (TIMA), Ilia Polian (Univ. of Passau), Elena Ioana Vatajelu (Politecnico di Torino)

11:15 – 11:30: Coffee Break

11:30 – 12:30: Special Session 3: Sensors for test and test instruments –Part 2

Organizer: H. Stratigopoulos (LIP6)

Moderator: H. Kobayashi (Gunma University)

- **Post-manufacturing "one-shot" calibration of analog/RF circuits based on non-intrusive sensors**
  Haralampos-G. Stratigopoulos, Sorbonne Universités, UPMC Univ. Paris 6, CNRS, LIP6, France
- **Temperature sensors to test analog circuits: FAQ**
  Antonio Rubio, Universitat Politècnica de Catalunya, Spain

12:30 – 13:45: Lunch

13:45 – 14:45: Regular session 3

Moderator: J. Machado da Silva (U. Porto)

- **Improving indirect test efficiency using multi-directional tessellations in the measure space**
  Alvaro Gomez-Pau, Luz Balado, Joan Figueras, Universitat Politècnica de Catalunya, Spain
- **Mostly-digital design of sinusoidal signal generators for mixed-signal BIST applications using harmonic cancellation**
  Hani Malloug, Manuel Barragan, Salvador Mir, Emmanuel Simeu, TIMA, France, Hervé Le-Gall, STMicroelectronics, France

1st IEEE International Verification and Security Workshop (IVSW)

Conference Room: Port Salvi

09:00 – 09:50: Session 7 – Keynote Address

- **Keynote Address:** Dr. Ulirch Rührmair, Ruhr-Universitat Bochum, **Physical Disorder for Hardware Security**

09:50 – 10:15: Break

11:30 – 12:30: Session 9 – Flaw detection and security verification

Moderator: Rajat Subhra Chakraborty, ITT Kharagpur India

- **MaskVer: A Tool Helping Designers Detect Flawed Masking Implementations**
  Michael Tempelmeier and Georg Sigl, Technische Universität München
- **On Fault Injections for Early Security Evaluation vs. Laser-based Attacks**
  Regis Leveugle, Amine Chahed, Paolo Maistri, Athanasios Papadimitriou, David Hély, Vincent Beroulle & Abdelaziz Ammari, Univ. Grenoble Alpes, ENISo

12:30 – 13:45: Lunch

13:45 – 14:45: Session 10 – Secure Verification

Moderator: Nejmeddine Alimi, Tunis Univ.

- **Secure Debug throughout the SoC life cycle**
  David Hely, Jerry Backer and Ramesh Karri, Univ. Grenoble Alpes, New York University
- **Using Outliers to Detect Stealthy Hardware Trojan Triggering**
  Papa-Sidy Ba, Sophie Dupuis, Marie-Lise Flottes, Giorgio Di Natale and Bruno Rouzeyre LIRMM

15:10 - 22:40: Social Event

Visit of Gaudi's Park Güell, and Diner

15:10: Departure of Buses from the hotel

22:40: Arrival of Buses to the hotel

Wednesday July 6, 2016

22nd IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS)

Conference Room: Mediterraneo

09:00 – 10:00: Session 8 – Fault Detection and Diagnosis

Moderator: N.-E.Zergainoh (TIMA)

- **Scalable FPGA Graph model to detect routing faults**
  L. Sterpone, G. Cabodi, S.F.Finocchiaro, C.Loiacono, F.Savarese, B.Du (Politecnico di Torino)
- **Concurrent Error Detection and Tolerance in Kalman Filters Using Encoded State and Statistical Covariance Checks**
  S.Pandey, S.Banerjee, A.Chatterjee (Georgia Institute of Technology)
- **Automatic Generation of Stimuli for Fault Diagnosis in IEEE 1687 Networks**
  R.Cantoro, M.Montazeri, M.Sonza Reorda (Politecnico Di Torino), F.Ghani Zadegan, E.Larsson (Lund U)

10:00 – 10:15: Break

10:15 – 11:15: Session 9 – Reliability Pot-Pourri

Moderator: L.Anghel (TIMA)

- **RIIF-2: toward the next generation Reliability Information Interchange Format**
  A.Savino, S.Di Carlo, A.Vallero, G.Politano (Politecnico di Torino), D.Gizopoulos (U Athens), A.Evans (iRoC)
- **STT-MTJ-based TRNG with On-The-Fly Temperature/Current Variation Compensation**
  E.Vatajelu (Politecnico di Torino)
  G.Di Natale (LIRMM), P.Prinetto (Politecnico di Torino)
- **SET Response of a SEL Protection Switch for 130 and 250 nm CMOS Technologies**
  M.Andjelkovic, A.Ilic (U Nis), V.Petrovic (IHP), M.Nenadovic (IHP), Z.Stamenkovic (IHP), G.Ristic (U Nis)

11:15 – 11:30: Coffee Break

11:30 – 12:30: Session 10 – Posters

- **Reusing Logic Masking to Facilitate Path-Delay-Based Hardware Trojan Detection**
  A.Nejat, D.Hely, V.Beroulle (Grenoble Alpes U)
- **Evaluation of machine learning algorithms for Image Quality Assessment**
  R.Alhakim, G.Takam Tchendjou, E.Simeu (TIMA Laboratory), F.Lebowsky (STMicroelectronics)
- **An Odd-Even Scheme to Prevent a Packet from Being Corrupted and Dropped in Fault Tolerant NoCs**
  B.Bhowmik, S.Biswas, J.K.Deka (IIT Guwahati)
- **Feasibility of Software-based Repair for Program Memories**
  P.Skoncej (BTU Cottbus-Senftenberg), F. Muhlbauer, F.Kubicek, L.Schroder, M.Scholzel (U of Potsdam)
- **Hardware Trojans Classification for Gate-level Netlists based on Machine Learning**
  K.Hasegawa, M.Oya, M.Yanagisawa, N.Togawa (Waseda U)
- **On the influence of compiler optimizations in the fault tolerance of embedded systems**
  A.Serrano-Cases, J.Isaza-Gonzalez, S.Cuenca-Asensi, A.Martinez-Alvarez (U Alicante)
- **Online Monitoring of NBTI and HCD in Beta-Multiplier Circuits**
  T.Hillebrand, M.Taddiken, K.Tscherkaschin, S.Paul, D.Peters-Drolshagen (U Breme
- **Online Monitoring of the Maximum Angle Error in AMR Sensors**
  A.Zambrano, H.Kerkhoff (U Twente)
- **Online Time Interference Detection in Mixed-Criticality Applications on Multicore Architectures using Performance Counters**
  S.Esposito, M.Violante (Politecnico di Torino), M.Sozzi, M.Terrone, M.Traversone (Finmeccanica)
- **Power-Side-Channel Analysis of Carbon Nanotube FET Based Design**
  C.K.H.Suresh, B.Mazumdar, S.S.Ali, O.Sinanoglu (New York U-Abu Dhabi)
- **Redesign for Untrusted Gate-level Netlists**
  M.OYA (Waseda U, NEC), M.Yanagisawa, N.Togawa (Waseda U)

12:30 – 13:45: Lunch

13:45 – 14:45: Session 11 – Robust Storage Elements

Moderator: A.Rubio (UPC)

- **Single-Event Performance of Differential Flip-Flop Designs and Hardening Implication**
  R.M.Chen (Tsinghua U), E.X.Zhang, B.L.Bhuva, L.W.Massengill, W.T.Holman (Vanderbilt U)
- **Conditional Soft-Edge Flip-Flop for SET Mitigation**
  P.Sismanoglou, D.Nikolos (U Patras)
- **A High Performance Scan Flip-Flop Design for Serial and Mixed Mode Scan Test**
  S.Ahlawat (IIT Bombay), J.Tudu (IIS Bangalore), A.Matrosova (Tomsk State U), V.Singh (IIT Bombay)

14:45 – 15:00: Break

15:00 – 16:00: Session 12 – Security

Moderator: E.Sanchez (Politecnico di Torino)

- **Binary decision diagram to design balanced secure logic styles**
  H.KIM (KU Leuven and iMinds), S.Hong (Korea U), B.Preneel, I.Verbauwhede (KU Leuven and iMinds)
- **A Hybrid Self-diagnosis Mechanism with Defective Nodes Locating and Attack Detection for Parallel Computing Systems**
  L.Bu, M.Karpovsky (Boston U)
- **Hardware Enlightening: No Where to Hide Your Hardware Trojans**
  M.S.Samimi, E.Aerabi, Z.Kazemi, M.Fazeli, A.Patooghy (Iran U of Science and Technology)

16:00: Symposium Closing Remarks

21st IEEE International Mixed Signal Testing Workshop (IMSTW)

Conference Room: Goya

09:00 – 10:00: Regular session 4

Moderator: A. Ginés (U. Sevilla)

- **Defect Diagnosis and localization methodology for pipelined ADCs**
  Mohamed Abbas, Ashraf Ramadan, Assiut University, Egypt
- **Determination of the Drift of the Maximum Angle Error in AMR Sensors Due to Aging**
  Andreina Zambrano, Hans Kerkhoff, University of Twente, Netherlands

10:00 – 10:15: Break

10:15 – 11:15: Invited talks 3

Moderator: A. Rubio (UPC)

- **A compact R-2R DAC for BIST applications**
  Antonio Rabal, Aranzazu Otin, Isidro Urriza, Universidad de Zaragoza, Spain, Antonio Jose Gines, Gildas Leger, Adoracion Rueda, IMSE-CNM, CSIC-Universidad de Sevilla, Spain
- **On-Chip Implementation of ECoG Signal Data Decoding in Brain-Computer Interface**
  Mradul Agrawal, Sandeep Vidyashankar, Ke Huang, San Diego State University

11:15 – 11:30: Coffee Break

11:30 – 12:30: Regular session 5

Moderator: F. Azaïs (LIRMM)

- **Authentication and security system based on optical variable nanostructures applied to CMOS processes and systems**
  Jasbir N Patel, Hao Jiang, Bozena Kaminska, Simon Fraser University, Canada
- **Common Pitfalls in Application of a Threshold Detection Comparator to a Continuous-Time Level Crossing Quantization**
  Takahiro Yamaguchi, Advantest Laboratories Ltd, Japan, Katsuhiko Degawa, Advantest Corporation, Japan, Tetsuya Iizuka, Kunihiro Asada, University of Tokyo, Japan

12:30 – 13:45: Lunch

13:45 – 14:15: Regular session 6

Moderator: TBD

- **Generation of a Comprehensive Final Test MSA**
  Eric Calip, Christian Argon Aranas, Mark Ramos, Texas Instruments, Philippines

14:15: Workshop Closing Remarks

1st IEEE International Verification and Security Workshop (IVSW)

Conference Room: Port Salvi

09:00 – 9:45: Session 11 – Distinguished Presentation

- **Distinguished Speaker:** Prof. Jacob Abraham, University of Texas at Austin, **Next Generation Intrusion Prevention,**
  Co-author: Amaya Chaudhari

9:45 – 10:15: Break

10:15 – 11:15: Session 12 – Design Debug and Diagnosis

Moderator: Jacob Abraham, UT Austin

- **Revision Debug with Non-Linear Version History in Regression Verification**
  John Adler, Ryan Berryhill and Andreas Veneris, University of Toronto
- **Counterexample-Guided Diagnosis**
  Heinz Riener and Goerschwin Fey, University of Bremen & German Aerospace Center (DLR)

11:15 – 11:30: Coffee Break

11:30 – 12:30: Session 13 - Technology Challenges and Innovations

Moderator: Andreas Veneris, U. Toronto

- **In-situ slack monitors: Taking up the challenge of on-die monitoring of variability and reliability**
  Ahmed Benhassain, ST Microelectronics
- **A Digital Memristor Emulator for FPGA-Based Artificial Neural Networks**
  Ioannis Vourkas, Vasileios Ntinas, Angel Abusleme, Georgios Ch. Sirakoulis and Antonio Rubio, Pontificia Universidad Catolica de Chile, Democritus University of Thrace, & Polytechnic University of Catalonia

12:30 – 13:45: Lunch

13:45 – 14:45: Session 14 – Secure Formal Verification

Moderator: Ahmed Benhassain, ST Micro

- **Generating Good Properties from a Small Number of Use Cases**
  Jan Malburg, Tino Flenker and Goerschwin Fey, University of Bremen & German Aerospace Center (DLR)
- **Secure Path Verification**
  Gianpiero Cabodi, Paolo Camurati, Sebastiano Fabrizio Finocchiaro, Carmelo Loiacono, Francesco Savarese and Danilo Vendraminetto, Politecnico di Torino

14:45: Workshop Closing Remarks